REMARKS

Applicant has made a number of changes to the specification, drawings and claims to correct minor inadvertent errors not affecting the content of the disclosure itself. Also, in the case of the claims, an error was noted in the description of the buck converter circuits in claim 22, which error was replicated in claims 32, 45-58, 60, 62 and 64. This error has been corrected herein. Each of these requested changes is discussed below.

With respect to Figure 2a, the change in the identification of the external resistor Rgane to Rgain is to conform the figure to the paragraph starting on line 47 of column 3, and specifically as identified in line 57 of column 3 of the patent. The addition of the three connection dots is to conform these connections to the connection convention otherwise used in the drawings, the connections themselves being clear from the fact that they are all "T" connections, and thus are clear connections with or without the dots. With respect to the requested changes to Figure 2b, a missing lead line has been added (see column 4 starting on line 18 of the patent, specifically identifying the amplifier as amplifier 68). Also, connection dots have been added at two additional "T" connections. With respect to Figure 2c, the missing portion of NAND gate 56 has been added in accordance with the conventional symbol used for NAND gates.

Note the reference to NAND gates 54 and 56 in column 3, line 37 of the original patent, as well as NAND gate 54 in Figure 2a of the other converter in the exemplary dual converter configuration. Also, four connection dots have been added at "T" connections. With respect to Figure 2d, the reference V has been added. The voltage V is an input voltage as shown in Figure 2b, with the description of the operation of transistor Q7 relative to the analog voltage V appearing in column 8, lines 5-14, making clear that the voltage V is applied to the base of transistor Q7.

With respect to the requested changes in the specification, the change in the paragraph that begins on column 3, line 47 to identify the node as node 64, rather than node 62, is supported by the associated description together with a reference to Figure 2a, wherein the amplifier is amplifier 62 and the node is node 64. With respect to the paragraph that begins on column 7, line 8, note the sentence starting on line 19 of column 7. This portion of the specification is obviously discussing the control of power devices N1 and P1, and N2 and P2, not N2 and P1. With respect to the requested change in the paragraph starting on line 50 of column 7, the change in the identification of the resistor from R16 to R18 is to conform the associated description in the specification with the identification of the resistor in Figure 2d. Finally, with respect to the requested change in the paragraph that begins on line 13 of column 8, the words "inverter" and "inverters" were inadvertently used, when

obviously this paragraph and the rest of the disclosure relate to interleaved "converters," not "inverters."

With respect to the changes in the claims, these changes are of two types. First, the word "current" has been changed in a number of places to the word "currents," and the words "duty cycle" have been changed in a number of places to the words "duty cycles," as simple grammatical changes. Also, in claim 22, the buck converters were inadvertently improperly characterized, which has now been corrected by the requested amendment. In particular, clearly in a buck converter, the inductor alternately conducts between the first power supply terminal and a common load, and the second power supply terminal and the common load, not as previously set forth. This error had been replicated in claims 32, 45-58, 60, 62 and 64, which claims have now been similarly corrected to conform the characterization of buck converters with the recitation of the buck converters as positive elements of the claims.

In addition, applicant has recently become aware of additional prior art, and accordingly is filing an Information Disclosure Statement concurrently herewith. This prior art discloses current balancing in multiphase boost converters, not buck converters. In that regard, it should be noted that the original claims are all limited to use of a single sense resistor, all new claims are now specifically limited to buck

converters and not boost converters, and all claims are limited to realization in integrated circuit form.

A Supplemental Reissue Oath/Declaration is being provided herewith. Also applicant stands ready to surrender the original patent upon confirmation of allowance of all claims in the reissue application.